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Electronic Version v1.1

Stylesheet Version v1.1.0

Title of
Invention

JITTER-RESISTIVE DELAY LOCK LOOP CIRCUIT FOR LOCKING DELAYED CLOCK AND METHOD THEREOF

Application Number:

Date:

First Named Applicant:

Jui-Hsing Tseng

Confirmation Number:

Attorney Docket Number:

MTKP0186USA

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Submitted By:	Elec. Sign.
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Registered Number: 41,526	

Documents being submitted:	Files
us-declaration	MTKP0186-0-A1-usdecl.xml
us-declaration	us-declaration.dtd
	us-declaration.cdd us-declaration.xsl
us-fee-sheet	MTKP0186-0-A1-usfees.xml
u5-166-51166t	us-fee-sheet.xsl
	us-fee-sheet.dtd
us nower of ottornou grant	MTKP0186-0-A1-uspoat.xml
us-power-of-attorney-grant	us-power-of-attorney-grant.dtd
	us-power-of-attorney-grant.xsl
us-ids	MTKP0186-0-A1-usidst.xml
u5-lu5	us-ids.dtd
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ua aggianment	MTKP0186-0-A1-usassn.xml
us-assignment	
	us-assignment.xsl us-assignment.dtd
	MTKP0186-0-A1ASS1.tif
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us-request	MTKP0186-0-A1-usrequ.xml
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us-declaration	MTKP0186-0-ATDEC1.til
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application-body	application-body.dtd
	Image1.tif
	Image10.tif
	Image10.tif
	Image11.tif
	Image13.tif
	Image14.tif
	Image15.tif
	Image 16.tif
	Image2.tif
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	Image4.tif
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	mathml2-qname-1.mod
	mmlalias.ent
	mmlextra.ent
	soextblx.dtd
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abstract-pdf	MTKP0186-0-A1-ABX-abst.pdf
claims-pdf	MTKP0186-0-A1-ABX-clms.pdf
description-pdf	MTKP0186-0-A1-ABX-desc.pdf
drawings-pdf	MTKP0186-0-A1-ABX-draw.pdf
Comments	